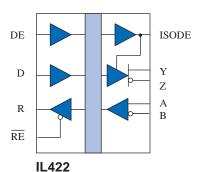


# Isolated RS422/RS485 Interface

#### **Functional Diagram**



**IL422 Receiver** 

RE	R	$V_{(A-B)}$
Н	Z	X
L	Н	≥ 200 mV
L	L	≤−200 mV
L	I	Open

## **IL422 Driver**

DE	D	$\mathbf{V_{(Y-Z)}}$
L	X	Z
Н	Н	≥ 200 mV
Н	L	≤−200 mV

H = High Level, L = Low LevelI = Indeterminate, X = Irrelevant, Z = High Impedance

#### **Features**

- 3.3 V Input Supply Compatible
- 2500 V<sub>rms</sub> Isolation (1 min.)
- 25 ns Maximum Propagation Delay
- 25 Mbps Data Rate
- 1 ns Pulse Skew (typ.)
- ±60 mA Driver Output Capability
- Thermal Shutdown Protection
- Meets or Exceeds ANSI 422-B, EIA 485-A and ITU Recommended V11
- Low EMC Footprint
- −40°C to +85°C Temperature Range
- PROFIBUS International Component Recognition
- 16-pin SOIC Package
- UL1577 and IEC 61010-2001 Approved

### **Applications**

Multi-point or multi-drop transmission on long bus lines in noisy environments.

#### **Description**

The IL422 is a galvanically isolated, high-speed differential bus transceiver, designed for bidirectional data communication on balanced transmission lines. The devices use NVE's patented\* IsoLoop spintronic Giant Magnetoresistance (GMR) technology. The IL422 is the first isolated RS-422 interface in a standard 16-pin SOIC package that meets the ANSI Standards EIA/TIA-422-B and RS-485 and is compatible with 3.3V input supplies.

The IL422 has current limiting and thermal shutdown features to protect against output short circuits and bus contention situations that could cause excessive power dissipation.



Absolute Maximum Ratings(11)

Parameters	Symbol	Min.	Тур.	Max.	Units	Test Conditions
Storage Temperature	$T_s$	-65		150	°C	
Ambient Operating Temperature	$T_{A}$	-40		100	°C	
Voltage Range at A or B Bus Pins		-7		12	V	
Supply Voltage <sup>(1)</sup>	$V_{\mathrm{DD1}}, V_{\mathrm{DD2}}$	-0.5		7	V	
Digital Input Voltage		-0.5		5.5	V	
Digital Output Voltage		-0.5		$V_{DD} + 1$	V	
Continuous Total Power Dissipation				725 377	mW	25°C 85°C
Maximum Output Current	$I_{o}$			95	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

**Recommended Operating Conditions** 

Parameters	Symbol	Min.	Тур.	Max.	Units	<b>Test Conditions</b>
Supply Voltage	$egin{array}{c} V_{ ext{DD1}} \ V_{ ext{DD2}} \end{array}$	3.0 4.5		5.5 5.5	V	
Input Voltage at any Bus Terminal (separately or common mode)	$egin{array}{c} oldsymbol{V_{I}} \ oldsymbol{V_{IC}} \end{array}$			12 -7	V	
High-Level Digital Input Voltage	$V_{\mathrm{IH}}$	2.4 3.0		$V_{DD1}$	V	$V_{DD1} = 3.3 \text{ V} $ $V_{DD1} = 5.0 \text{ V}$
Low-Level Digital Input Voltage	$V_{\scriptscriptstyle \rm IL}$	0		0.8	V	
Differential Input Voltage <sup>(2)</sup>	$ m V_{ID}$			±12	V	
High-Level Output Current (Driver)	$I_{\mathrm{OH}}$			60	mA	
High-Level Digital Output Current (Receiver)	$I_{OH}$			8	mA	
Low-Level Output Current (Driver)	$I_{OL}$	-60			mA	
Low-Level Digital Output Current (Receiver)	$I_{OL}$	-8			mA	
Ambient Operating Temperature	$T_{A}$	-40		85	°C	
Transient Immunity	·	20			kV/μs	
Digital Input Signal Rise and Fall Times	$t_{\rm IR}, t_{\rm IF}$			DC S	table	

**Insulation Specifications** 

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Parameters	Symbol	Min.	Тур.	Max.	Units	Test Conditions
Creepage Distance		8.08				mm
Barrier Impedance			>10 <sup>14</sup>   7			$\Omega \parallel pF$
Leakage Current			0.2		μA	240 V <sub>RMS</sub> , 60 Hz

# **Safety and Approvals**

## IEC61010-1

TUV Certificate Numbers: N1502812, N1502812-101

Classification: Reinforced Insulation

Model	Package	Pollution Degree	Material Group	Max. Working Voltage
IL422	0.3" SOIC	II	III	$300  \mathrm{V}_{\mathrm{RMS}}$

# **UL 1577**

Component Recognition Pprogram File Number: E207481

Rated 2500V<sub>RMS</sub> for 1 minute

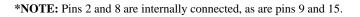
## **Soldering Profile**

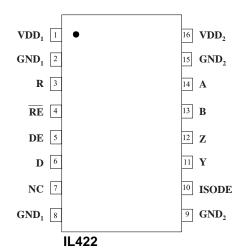
Per JEDEC J-STD-020C, MSL=2



# **IL422 Pin Connections**

1	$V_{DD1}$	Input Power Supply
2	$GND_1$	Input Power Supply Ground Return*
3	R	Output Data from Bus
4	RE	Read Data Enable (if $\overline{RE}$ is high, R = high impedance)
5	DE	Drive Enable
6	D	Data Input to Bus
7	NC	No Internal Connection
8	$GND_1$	Input Power Supply Ground Return*
9	$GND_2$	Output Power Supply Ground Return*
10	ISODE	Isolated DE Output for use in Profibus applications where the state of the isolated drive enable node needs to be monitored
11	Y	Y Bus (Drive – True)
12	Z	Z Bus (Drive – Inverse)
13	В	B Bus (Receive – Inverse)
14	A	A Bus (Receive – True)
15	$GND_2$	Output Power Supply Ground Return*
16	$V_{DD2}$	Output Power Supply







#### **Driver Section**

Electrical specifications are  $T_{min}$  to  $T_{max}$  and  $V_{DD} = 4.5 \text{ V}$  to 5.5 V unless otherwise stated.

Parameters	Symbol	Min.	Typ. <sup>(5)</sup>	Max.	Units	<b>Test Conditions</b>
Input Clamp Voltage	$V_{IK}$			-1.5	V	$I_L = -18 \text{ mA}$
Output voltage	V <sub>o</sub>	0		6	V	$I_0 = 0$
Differential Output Voltage <sup>(2)</sup>	$ V_{OD1} $	1.5		6	V	$I_0 = 0$
Differential Output Voltage <sup>(2)</sup>	$ V_{OD2} $	1.5	2.5	5	V	$R_L = 54 \Omega, V_{DD} = 5 V$
Differential Output Voltage <sup>(2)(6)</sup>	$V_{\mathrm{OD3}}$	1.5		5	V	$R_{L} = 54 \Omega, V_{DD} = 4.5 V$
Change in Magnitude of Differential Output Voltage <sup>(7)</sup>	$\Delta  V_{\scriptscriptstyle OD} $			±0.2	V	$R_L = 54 \Omega \text{ or } 100 \Omega$
Common Mode Output Voltage	V <sub>oc</sub>			3 -1	V	$R_L = 54 \Omega \text{ or } 100 \Omega$
Change in Magnitude of Common Mode Output Voltage <sup>(7)</sup>	$\Delta  V_{ m oc} $			±0.2	V	$R_L = 54 \Omega \text{ or } 100 \Omega$
Output Current <sup>(4)</sup> Output Disabled	$I_{o}$			1 -0.8	mA	$V_o = 12 \text{ V}$ $V_o = -7 \text{ V}$
High Level Input Current	${ m I}_{ m IH}$			10	μΑ	$V_{I} = 3.5 \text{ V}$
Low Level Input Current	${ m I}_{ m IL}$			-10	μΑ	$V_{I} = 0.4 \text{ V}$
				250		$V_0 = -6 \text{ V}$
Short-circuit Output Current	$I_{os}$			-150	mA	$V_0 = 0 V$
				-250		$V_0 = 8 \text{ V}$
Supply Current $V_{DD1} = +5 \text{ V}$	$I_{DD1}$		4	6	mA	No Load
Supply Current $V_{DD1} = +3.3 \text{ V}$	$I_{ m DD1}$		3	3	1117 \$	(Outputs Enabled)
		Switching Spe				
Parameters	Symbol	Min.	Typ. <sup>(5)</sup>	Max.	Units	Test Conditions
Maximum Data Rate		25			Mbps	$R_L = 54 \Omega, C_L = 50 \text{ pF}$
Differential Output Prop Delay	$t_D(OD)$		16	25	ns	$R_{L} = 54 \Omega, C_{L} = 50 \text{ pF}$
Pulse Skew <sup>(10)</sup>	$t_s(P)$		1	6	ns	$R_{L} = 54 \Omega, C_{L} = 50 pF$
Differential Output Rise & Fall Time	$t_{T}(OD)$		8	10	ns	$R_{L} = 54 \Omega, C_{L} = 50 pF$
Output Enable Time to High Level	$t_{\rm PZH}$		31	65	ns	$R_L = 54 \Omega, C_L = 50 pF$
Output Enable Time to Low Level	$t_{ m PZL}$		22	35	ns	$R_L = 54 \Omega, C_L = 50 pF$
Output Disable Time from High Level	$t_{ m PHZ}$		28	50	ns	$R_{L} = 54 \Omega, C_{L} = 50 pF$
Output Disable Time from Low Level	$t_{\scriptscriptstyle PLZ}$		16	32	ns	$R_L = 54 \Omega, C_L = 50 pF$
Skew Limit <sup>(3)</sup>	t <sub>sk</sub> (LIM)		2	8	ns	$R_L = 54 \Omega, C_L = 50 pF$

## Notes (apply to both driver and receiver sections):

- 1. All voltage values are with respect to network ground except differential I/O bus voltages.
- 2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
- 3. Skew limit is the maximum propagation delay difference between any two devices at 25°C.
- 4. The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
- 5. All typical values are at  $V_{DD1}$ ,  $V_{DD2} = 5$  V or  $V_{DD1} = 3.3$  V and  $T_A = 25$ °C.
- 6. The minimum  $V_{\text{OD2}}$  with a 100  $\Omega$  load is either ½  $V_{\text{OD1}}$  or 2 V, whichever is greater.
- 7.  $\Delta |V_{OD}|$  and  $\Delta |V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed form one logic state to the other.
- 8. This applies for both power on and power off, refer to ANSI standard RS-485 for exact condition. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.
- 9. Includes 8 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
- 10. Pulse skew is defined as  $|t_{PLH} t_{PHL}|$  of each channel.
- 11. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 6.
- 12. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 6).



## **Receiver Section**

Electrical specifications are $T_{min}$ to $T_{max}$	nd $V_{DD} = 4.5 \text{ V}$ to 5.5 V unless otherwise stated.
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Parameters	Symbol	Min.	Typ. <sup>(5)</sup>	Max.	Units	<b>Test Conditions</b>
Positive-going Input	•		-JF-			$V_0 = 2.7 \text{ V},$
Threshold Voltage	$V_{{\scriptscriptstyle IT+}}$			0.2	V	$I_0 = -0.4 \text{ mA}$
Negative-going Input	N/	-0.2			V	$V_0 = 0.5 \text{ V},$
Threshold Voltage	$V_{\text{IT-}}$	-0.2			V	$I_0 = 8 \text{ mA}$
Hysteresis Voltage (V <sub>IT+</sub> – V <sub>IT-</sub> )	$V_{HYS}$		60		mV	
High Level Digital Output Voltage	$V_{\text{OH}}$	$V_{DD} - 0.2$			V	$V_{\text{ID}} = 200 \text{ mV}$ $I_{\text{OH}} = -20  \mu\text{A}$
Low Level Digital Output Voltage	$V_{\text{OL}}$			0.2	V	$V_{ID} = -200 \text{ mV}$ $I_{OH} = 20  \mu\text{A}$
High-impedance-state output current	$I_{OZ}$			±10	μΑ	$V_0 = 0.4 \text{ to } (V_{DD2} - 0.5) \text{ V}$
Line Input Current <sup>(8)</sup>	$I_{I}$			1 -0.8	mA	$V_{I} = 12 \text{ V}$ $V_{I} = -7 \text{ V}$ $Other \text{ Input}^{(11)} = 0 \text{ V}$
Input Resistance	$r_{\rm I}$	12	20		kΩ	
Supply Current	$I_{DD2}$		27	34	mA	No load Outputs Enabled
	Swi	tching Charact				
Parameters	Symbol	Min.	<b>Typ.</b> <sup>(5)</sup>	Max.	Units	Test Conditions
Maximum Data Rate		25			Mbps	$R_L = 54 \Omega$ , $C_L = 50 pF$
Propagation Delay <sup>(9)</sup>	$t_{ m PD}$		24	32	ns	$V_0 = -1.5 \text{ V to } 1.5 \text{ V},$ $C_L = 15 \text{ pF}$
Pulse Skew <sup>(10)</sup>	$t_{sk}(P)$		1	6	ns	$V_0 = -1.5 \text{ V to } 1.5 \text{ V},$ $C_L = 15 \text{ pF}$
Skew Limit <sup>(3)</sup>	t <sub>sk</sub> (LIM)		2	8	ns	$R_L = 54 \Omega, C_L = 50 \text{ pF}$
Output Enable Time To High Level	$t_{PZH}$		17	24	ns	$C_L = 15 \text{ pF}$
Output Enable Time To Low Level	$t_{ m PZL}$		30	45	ns	$C_L = 15 \text{ pF}$
Output Disable Time From High Level	$t_{ m PHZ}$		30	45	ns	$C_L = 15 \text{ pF}$
Output Disable Time From Low Level	$t_{PLZ}$		18	27	ns	$C_L = 15 \text{ pF}$
		ching Characte	ristics at 3.3 V			
Parameters	Symbol	Min.	Typ. (5)	Max.	Units	Test Conditions
Maximum Data Rate		25			Mbps	$R_L = 54 \Omega, C_L = 50 pF$
Propagation Delay <sup>(9)</sup>	$t_{ m PD}$		27	32	ns	$V_o = -1.5 \text{ V to } 1.5 \text{ V},$ $C_L = 15 \text{ pF}$
Pulse Skew <sup>(10)</sup>	$t_{sk}(P)$		2	6	ns	$V_0 = -1.5 \text{ V to } 1.5 \text{ V},$ $C_L = 15 \text{ pF}$
Skew Limit <sup>(3)</sup>	$t_{sk}(LIM)$		4	8	ns	$R_L = 54 \Omega, C_L = 50 pF$
Output Enable Time To High Level	$t_{ m PZH}$		20	24	ns	$C_L = 15 \text{ pF}$
Output Enable Time To Low Level	$t_{PZL}$		33	45	ns	$C_L = 15 \text{ pF}$
Output Disable Time From High Level	$t_{ m PHZ}$		33	45	ns	$C_L = 15 \text{ pF}$
Output Disable Time From Low Level	$t_{ m PLZ}$		20	27	ns	$C_L = 15 \text{ pF}$

Magnetic Field Immunity(11)

Magnetic Field Immunity at 5 V						
Power Frequency Magnetic Immunity	$H_{PF}$	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	$H_{PM}$	4000	4500		A/m	$t_p = 8\mu s$
Damped Oscillatory Magnetic Field	$H_{OSC}$	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier (12)	$K_X$		2.5			
	Magn	etic Field Imr	nunity at 3.3 V	V		
Power Frequency Magnetic Immunity	$H_{PF}$	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	$H_{PM}$	1800	2000		A/m	$t_p = 8\mu s$
Damped Oscillatory Magnetic Field	$H_{OSC}$	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(12)</sup>	K <sub>X</sub>		2.5			



## **Application Information**

### **Electrostatic Discharge Sensitivity**

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

## **Electromagnetic Compatibility**

The IL422 is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

EN50081-1

Residential, Commercial & Light Industrial

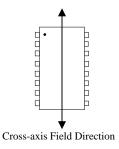
Methods EN55022, EN55014

EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field) ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



#### **Dynamic Power Consumption**

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on frequency and time.

The approximate power supply current per channel is:

$$I_{IN} = 40 \text{ x} \frac{f}{f_{MAX}} \text{ x} \frac{1}{4} \text{ mA}$$

Where f =operating frequency

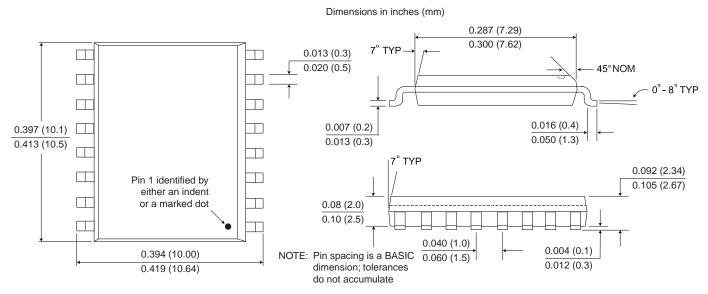
$$f_{\text{MAX}} = 50 \text{ MHz}$$

#### **Power Supply Decoupling**

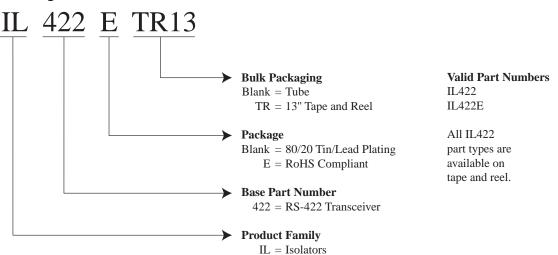
Low ESR capacitors such as ceramic are required to decouple the supplies. Both  $V_{DD1}$  and  $V_{DD2}$  must be bypassed with 47 nF capacitors. These should be placed as close as possible to  $V_{DD}$  pins for proper operation. Additionally,  $V_{\,DD2}$  should have a 10  $\mu F$  tantalum capacitor connected in parallel with the 47 nF capacitor.



# 0.3" 16-pin SOIC Package



# **Ordering Information and Valid Part Numbers**



RoHS COMPLIANT



ISB-DS-001-IL422-P	Changes
June 2011	Added clarification of internal ground connections.
ISB-DS-001-IL422-O	Changes
	Added low EMC footprint.
ISB-DS-001-IL422-N	Changes
	• Added magnetic field immunity and electromagnetic compatibility specifications.
	Added note on package drawing that pin-spacing tolerances are non-accumulating.
ISB-DS-001-IL422-M	Changes
	• Changed ordering information to reflect that devices are now fully RoHS compliant with no exemptions.
ISB-DS-001-IL422-L	Changes
	Reorganized supply current specifications; misc. minor changes
ISB-DS-001-IL422-K	Changes
	Eliminated soldering profile chart
ISB-DS-001-IL422-J	Changes
	• Updated open input state in truth table
ISB-DS-001-IL422-I	Changes
	Updated package drawing; misc.
ISB-DS-001-IL422-H	Changes
	Updated UL and IEC approvals
ISB-DS-001-IL422-G	Changes
	Revision letter added.
	Ordering Information Removed.
	• IEC 61010-1 Classification: "Reinforced Insulation" added.
	Notes added.
	IR Soldering Profile added
	Ordering Information added.



#### **About NVE**

An ISO 9001 Certified Company

NVE Corporation manufactures innovative products based on unique spintronic Giant Magnetoresistive (GMR) technology. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometers), Digital Magnetic Field Sensors, Digital Signal Isolators, and Isolated Bus Transceivers.

NVE pioneered spintronics and in 1994 introduced the world's first products using GMR material, a line of ultra-precise magnetic sensors for position, magnetic media, gear speed and current sensing.

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Specifications shown are subject to change without notice.

ISB-DS-001-IL422-P

June 2011